WHAT IS CLAIMED IS:

1. A vertical transistor architecture comprising:

an array of vertical transistor cells formed in a substrate and arranged in a transistor plane, in rows in an x direction, and in columns in a y direction perpendicular to the x direction;

an array of active trenches, wherein the active trenches separate the rows of transistor cells; and

an array of isolation trenches, wherein the isolation trenches separate the columns of transistor cells;

wherein the active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction.

2. The vertical transistor architecture of claim 1, wherein the vertical transistor cells comprise:

respective lower source/drain connection region;

respective upper source/drain connection regions arranged above the lower source drain regions;

respective conductive channels disposed between the upper and lower source/drain connection regions; and

respective gate electrodes insulated from the active regions by a gate dielectric.

3. The vertical transistor architecture of claim 2, wherein the gate electrodes are arranged in the active trenches and wherein the gate electrodes of transistor cells which are adjacent in the x direction are connected to one another and form sections of word lines.

4. The vertical transistor architecture of claim and 2, wherein the lower source/drain connection regions are in each case connected to a contiguous connection plate.

5. The vertical transistor architecture of claim 2, wherein the lower source/drain connection regions are in each case sections of a connection plate that is patterned at least in an upper region and is contiguous in a lower region.

6. The vertical transistor architecture of claim 2,

wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction.

7. The vertical transistor architecture of claim 6, further comprising a plurality of layer bodies deposed in the transistor cell array and in each case separated from one another by the active trenches.

8. The vertical transistor architecture of claim 7, wherein the layer bodies are lengthened in each case row by row into a connection array adjoining the transistor cell array.

9. The vertical transistor architecture of claim 8, wherein the layer bodies are connected to one another in the region of the connection array.

10. The vertical transistor architecture of claim 6, wherein the layer bodies are connected to a structure having a substrate potential.

11. The vertical transistor architecture of claim 6, wherein the connection plate is patterned in an upper region by the active trenches extending along the x axis, wherein the lower source/drain connection regions are formed in the upper region of the connection plate in each case below the active regions, wherein the isolation trenches have a smaller depth than the active trenches, and wherein the layer bodies are formed contiguously row by row in each case in a lower region below the isolation trenches.

12. The vertical transistor architecture of claim 11, wherein the isolation trenches are filled with an insulator material.

13. The vertical transistor architecture of claim 6, wherein the isolation trenches and the active trenches have an essentially identical depth, wherein the lower source/drain connection regions are formed in each case in an upper region of the connection plate below the active trenches, and wherein the layer bodies are formed contiguously row by row in each case below the active regions and are separated from one another by the source/drain connection regions in a lower region.

14. The vertical transistor architecture of claim 6, wherein an upper region of the connection plate is patterned in the x direction and in the y direction, wherein a lower source/drain connection region delimited in the x direction and the y direction is in each case formed in the

upper region of the connection plate, and wherein the active regions of transistor cells which are adjacent in the x direction and the y direction are formed contiguously by a single layer body which is patterned by the lower source/drain connection regions.

15. The vertical transistor architecture of claim 14, wherein the layer body is lengthened into a connection array adjoining the transistor cell array.

16. The vertical transistor architecture of claim 14 , wherein the layer body is connected to a structure having a substrate potential.

17. The vertical transistor architecture of claim 2, wherein the active regions of the transistor cells have a cross-sectional area of essentially F^2 relative to a production-dictated minimum feature size F parallel to the transistor plane, and wherein the area requirement of a transistor cell is essentially 4 F^2.

18. The vertical transistor architecture of claim 2, further comprising a storage capacitor electrically connected to a source/drain connection region of each selection transistor, whereby an array of memory cells each containing a vertical selection transistor is formed.

19. The vertical transistor architecture of claim 18, wherein the selection transistors are connected to the assigned storage capacitor in each case at an upper source/drain connection region.

20. A method for fabricating vertical transistor cells in a substrate comprising:

arranging the transistor cells in rows along an x direction and in columns along a y direction perpendicular to the x direction;

providing a conductive connection plate in the substrate;

providing a precursor layer body on the conductive connection plate;

introducing isolation trenches extending along the y direction into an upper region of the precursor layer body;

forming active trenches which cut through the precursor layer body and pattern the connection plate in an upper region therein;

forming layer bodies separated by the active trenches from the precursor layer body;

forming lower source/drain connection regions from the upper regions of the connection plate; and

forming active regions of the transistor cells in the upper regions of the layer bodies, wherein the active regions are contiguous due to connection row by row being through the lower regions of the layer bodies.

21. The method of claim 20, wherein the connection plate is provided in the substrate as a layer of a first conduction type, and wherein the precursor layer body is provided as a layer of a second conduction type, opposite to the first conduction type, arranged on the connection plate.

22. The method of claim 21, wherein an n conduction type is provided as the first conduction type and a p conduction type is provided as the second conduction type, wherein the connection

plate is arranged from a heavy n-type doping of a layer of the substrate, and wherein the precursor layer body is arranged on the connection plate by epitaxy.

23. A method for fabricating vertical transistor cells in a substrate, wherein the transistor cells are arranged, in a transistor cell array, in rows along an x direction and in columns along a y direction perpendicular to the x direction, comprising:

providing a conductive connection plate in the substrate;

providing a precursor layer body on the conductive connection plate;

introducing active trenches running along the x direction and having a first width into an upper region of the precursor layer body;

forming lower source/drain connection regions extending as far as the connection plate in each case in sections of the precursor layer body that are arranged below the active trenches;

forming layer bodies that are separated from one another by the active trenches from the precursor layer body; and

forming active regions of the transistor cells row by row from the upper regions of the layer bodies, wherein the active regions are connected to one another by means of the lower regions of the layer bodies.

24. The method of claim 23, wherein the lower source/drain connection regions are formed selectively in sections of the precursor layer body that are arranged below the active trenches, comprising:

introducing isolation trenches running along the y direction and having a second width, which is less than the first width, into the respective upper regions of the layer bodies;

delimiting the transistor webs arising in the upper region of the layer bodies by the active trenches and the isolation trenches;

depositing a non conformal working layer that grows more rapidly on the transistor webs than in the active trenches and the isolation trenches; and

terminating the deposition process as soon as sections of the isolation trenches that lie between transistor webs adjacent in the x direction are covered by the working layer.

25. The method of claim 24, wherein the lower source/drain connection regions are formed by means of an ion implantation of the layer body, wherein the lower source/drain connection regions extend as far as the connection plate are formed in the sections of the layer body situated below the active trenches, and wherein the active regions of transistor cells adjacent in the x direction are connected by sections of the layer body situated below the transistor webs.

26. A method for fabricating vertical transistor cells in a substrate comprising:

arranging the transistor cells in a transistor cell array, in rows along an x direction and in columns along a y direction perpendicular to the x direction;

providing a conductive connection plate in the substrate;

patterning the connection plate in an upper region;

delimiting a lower source/drain connection region in the x direction and the y direction within the upper region of the connection plate;

arranging a contiguous layer body on the connection plate, patterned by the lower source/drain connection regions; and

forming active regions of the transistor cells in an upper region of the layer body, wherein the active regions of transistor cells adjacent in the x direction and the y direction are formed contiguously by means of the lower region of the layer body.

27. The of claim 26, wherein the connection plate is provided in the substrate as a layer of a first conduction type.

28. The method as claimed in claim 27, wherein an n conduction type is provided as the first conduction type, and wherein the connection plate is formed from a heavy n-type doping of a layer of the substrate.

29. The method of claim 26, wherein the patterning of the upper region of the connection plate comprises:

growing a first portion of the layer body epitaxially;

doping sections of the first portion of the layer body in accordance with the conductivity type of the connection plate, wherein the lower source/drain connection regions emerge from the doped sections of the layer body; and

epitaxially growing the second portion of the layer body.

30. The method of claim 26, wherein the doping is performed by a plurality of implantation steps having a different implantation energy.

31. The method of claim 26, wherein active trenches extending in the x direction are introduced into the layer body, wherein transistor webs are produced between the active trenches, and wherein the lower source/drain connection regions adjacent in the x direction are assigned to a transistor web and adjoin the assigned transistor web.

32. The method of claim 26, wherein the lower source/drain connection regions are provided in a manner projecting into the assigned transistor web.

33. The method of claim 26, wherein the lower source/drain connection regions are formed in conical fashion.